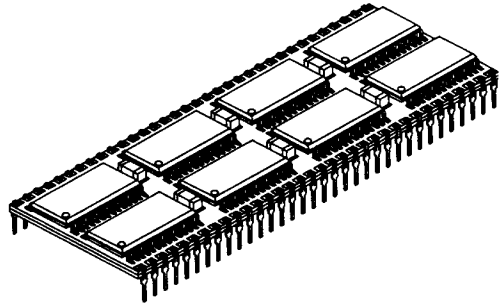


DESCRIPTION:

The DPS96122 is a four megabit Static Random Access Memory (SRAM), complete with decoupling capacitors. It can be organized as 256K X 16 or as 512K X 8.

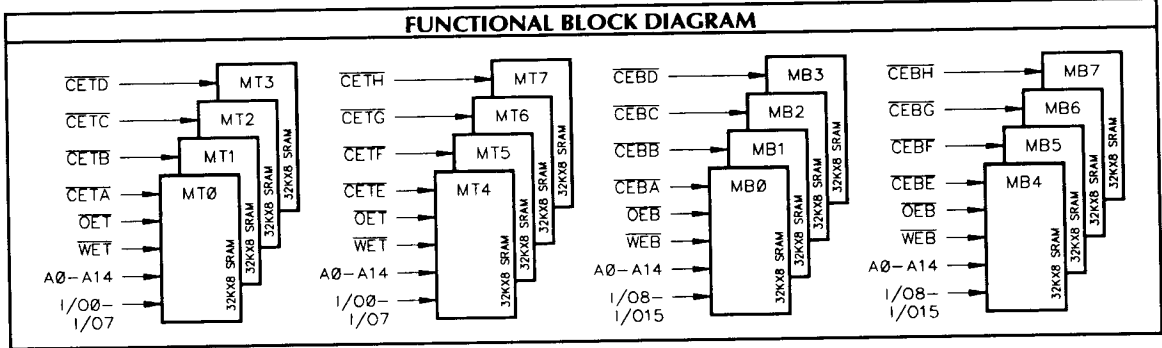
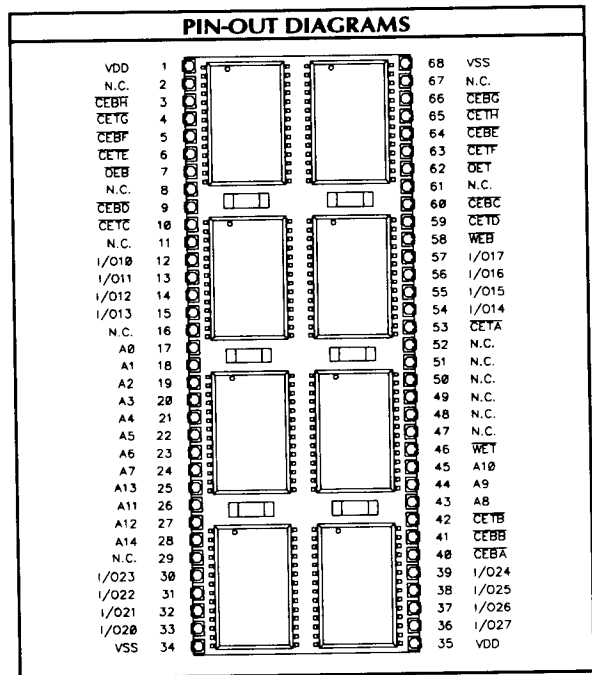
The DPS96122 is ideally suited for large memory applications where low power and ease of use is required.



4

FEATURES:

- Fast Access Times: 85, 100, 120, 150ns (max.)
- Faster Speed Available Upon Request
- Fully Static Operation; No Clock or Refresh Required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Input and Output
- Low Data Retention Voltage: 2.0V min.
- Standard 68-Pin DIP Package



PIN NAMES	
A0 - A19	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CE}TA$ - $\overline{CE}TH$	Chip Enables Top
$\overline{CE}BA$ - $\overline{CE}BH$	Chip Enables Bottom
$\overline{WE}T$	Write Enable Top
$\overline{WE}B$	Write Enable Bottom
$\overline{OE}T$	Output Enable Top
$\overline{OE}B$	Output Enable Bottom
VDD	Power (+5V)
VSS	Ground
N.C.	No Connect

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-50 to + 100	°C
T _{BIAS}	Temperature Under Bias	-40 to + 85	°C
V _{DD}	Supply Voltage ¹	-0.5 to + 7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} + 0.5	V

RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	160	pF	V _{IN} = 0V
C _{CE}	Chip Enable	160		
C _{WE}	Write Enable	80		
C _{OE}	Output Enable	160		
C _{I/O}	Data Input/Output	80		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4	-	V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA	-	0.4	V

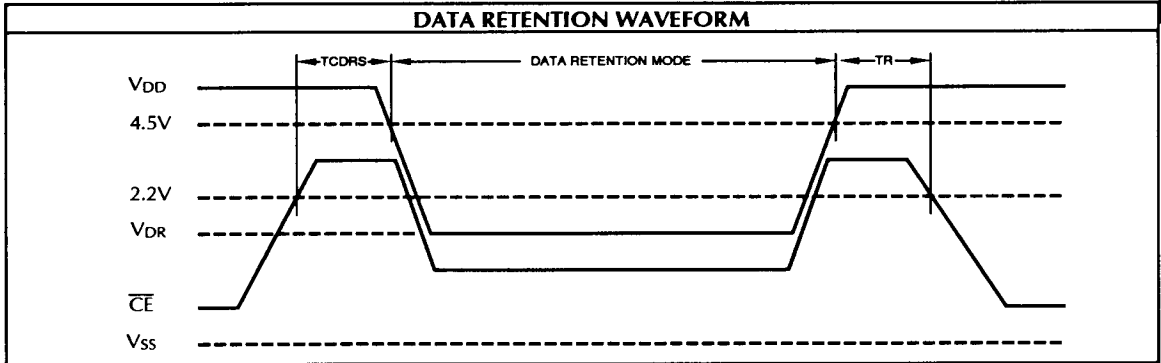
TRUTH TABLE					
Mode	\overline{CE}	\overline{WE}	\overline{OE}	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active

H = HIGH L = LOW X = Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	C		I		Unit
			Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-20	+20	-20	+20	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , \overline{CE} or \overline{OE} = V _{IH} , or \overline{WE} = V _{IL}	-20	+20	-20	+20	μA
I _{CC1}	Active Supply Current	\overline{CE} = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		75 (120)		75 (120)	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA		100 (170)		100 (170)	mA
I _{SB1}	Full Standby Supply Current	See Note 5		1.6		3.2	mA
I _{SB2}	Standby Supply	\overline{CE} = V _{IH}		32		32	mA
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2V		0.50		0.65	mA
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3V		0.65		0.80	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA		2.4		2.4	V

NOTE: Characteristics listed in parentheses are listed for the 256K x 16 organization when they differ from the 512K x 8 organization.

DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DD} - 0.2V$	2.0	5.0	5.5	V
t _{CDR}	Chip Disable to Data Retention Time		0			ns
t _R	Recovery Time	t _{RC} = Read Cycle Timing	t _{RC}			ns



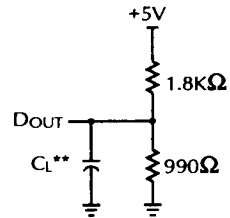
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition measured from 0.8V and 2.2V.

AC TEST CONDITIONS		
Load	C _L	Parameters Measured
1	100pF	except t _{CLZ} , t _{CHZ} , t _{WHZ} , t _{WLZ} , t _{OLZ} and t _{OHZ}
2	5pF	t _{CLZ} , t _{CHZ} , t _{WHZ} , t _{WLZ} , t _{OLZ} and t _{OHZ}

Figure 1. Output Load

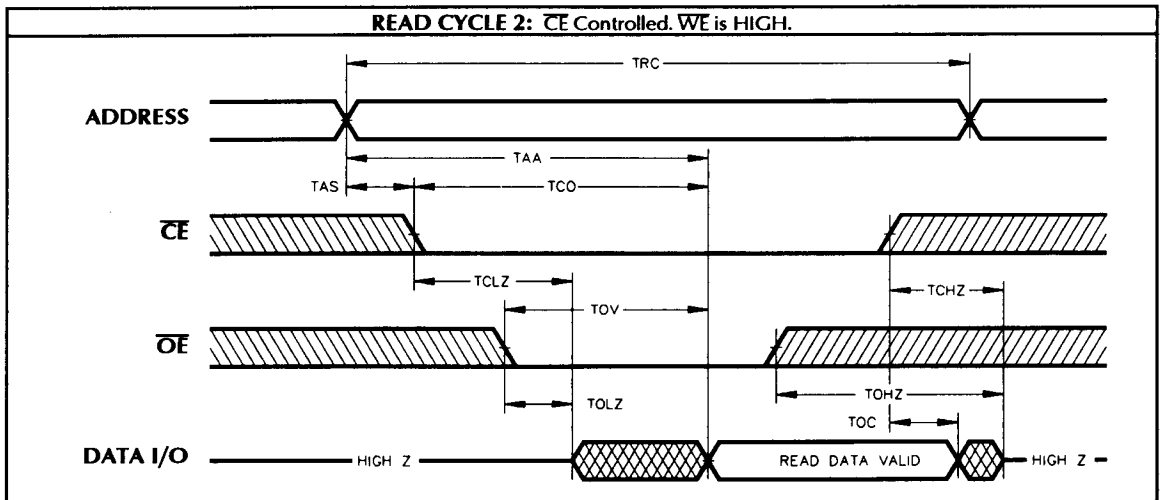
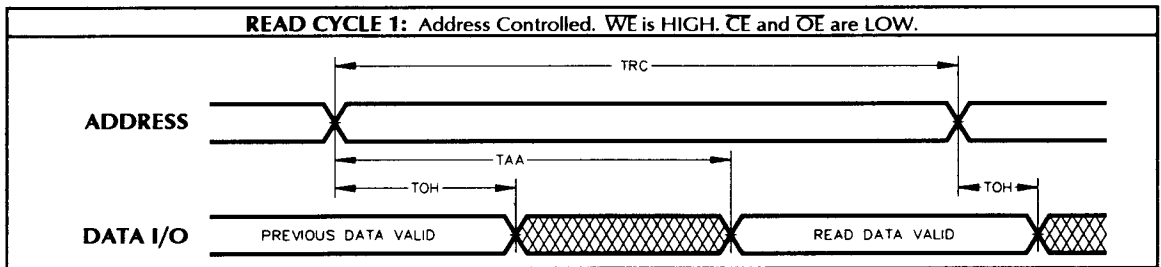
** Including Probe and jig Capacitance.

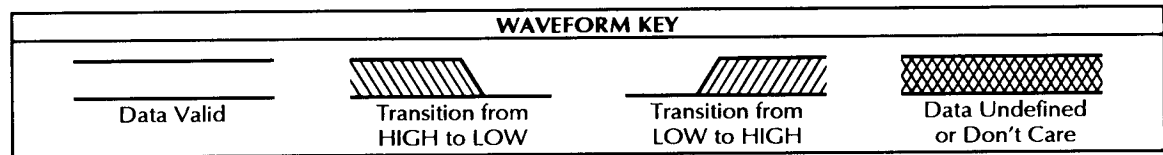
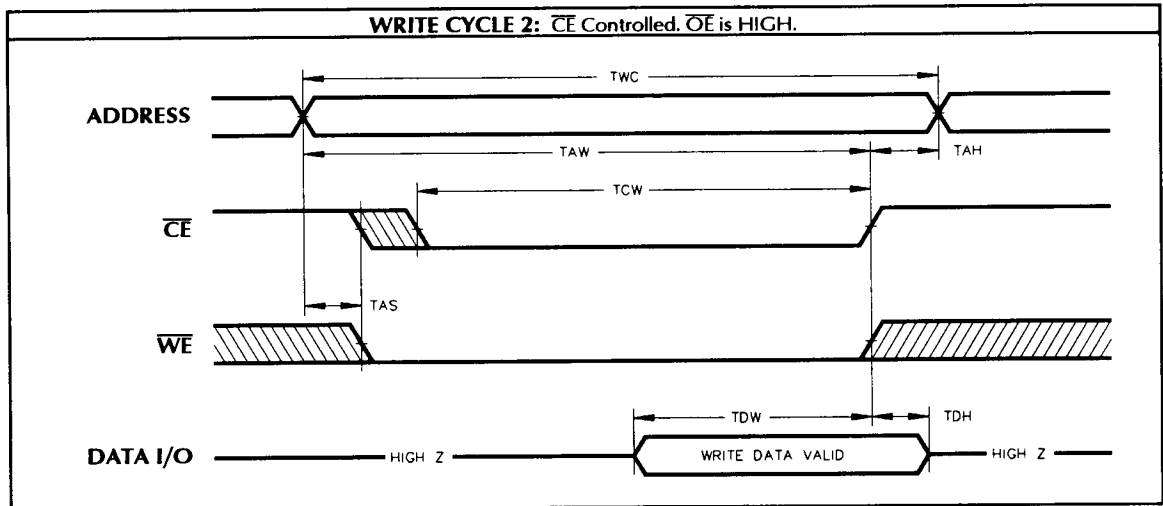
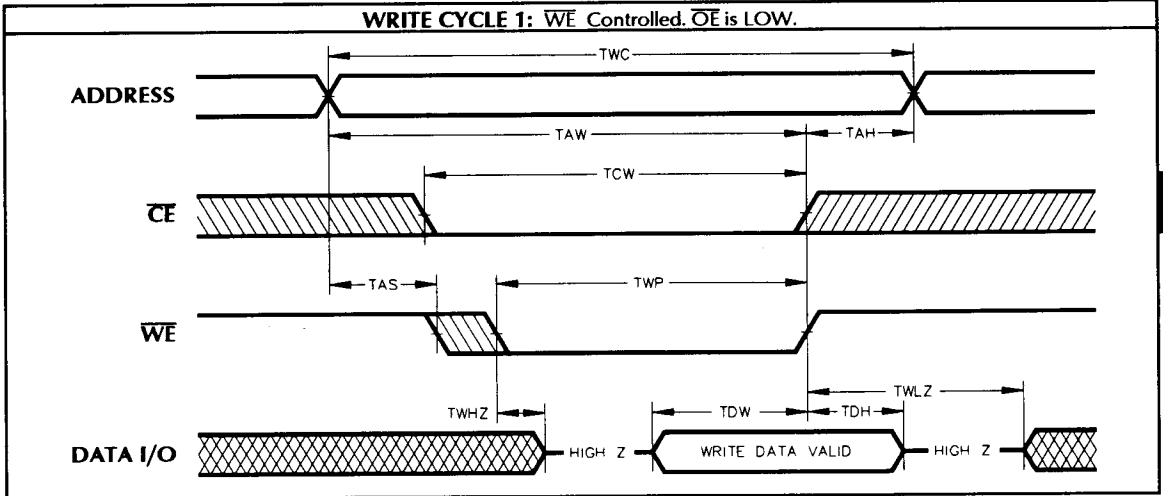


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	85		100		120		150		ns
2	t _{AA}	Address Access Time		85		100		120		150	ns
3	t _{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t _{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t _{OH}	Output Hold from Address Change	3		10		10		10		ns
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{6,7}	10		10		10		10		ns
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{6,7}	3		5		5		5		ns
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{6,7}		35		40		45		55	ns
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{6,7}		30		35		40		50	ns
10	t _{OC}	Output Hold from Chip Enable	0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁸											
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
11	t _{WC}	Write Cycle Time	85		100		120		150		ns
12	t _{AW}	Address Valid to End of Write	75		90		100		120		ns
13	t _{CW}	Chip Enable to End of Write	75		90		100		120		ns
14	t _{DW}	Data Valid to End of Write	35		40		50		60		ns
15	t _{DH}	Data Hold Time	0		0		0		0		ns
16	t _{WP}	Write Pulse Width	65		75		90		110		ns
17	t _{AS}	Address Set-up Time ***	0		0		0		0		ns
18	t _{AH}	Address Hold Time	5		5		5		5		ns
19	t _{WHZ}	Write Enable to Output in HIGH-Z ^{6, 7}		35		40		45		55	ns
20	t _{WLZ}	Write Enable to Output in LOW-Z ^{6, 7}	5		5		5		5		ns

*** Valid for both Read and Write Cycles.





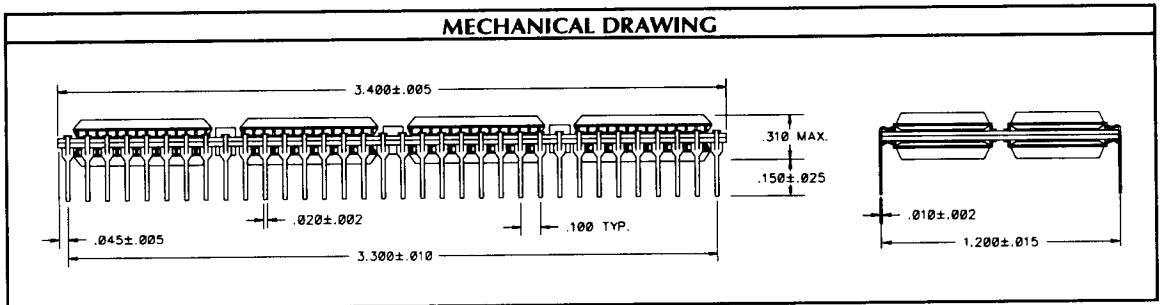
ORDERING INFORMATION

DP PREFIX	S96122 DEVICE TYPE	XXX SPEED	X GRADE			
				C	COMMERCIAL	0°C to +70°C
				I	INDUSTRIAL	-40°C to +85°C
		85			85ns	
		100			100ns	
		120			120ns	
		150			150ns	
					256Kx16 OR 512Kx8 CMOS SRAM MODULE	

NOTES:

1. All voltages are with respect to V_{ss}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. This parameter is measured with specified loading in Figure 1.
7. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
8. The outputs are in a high impedance state when \overline{WE} is LOW.

MECHANICAL DRAWING



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